Amendment to the claims:

1-10. (Canceled).

11. (Currently amended) An information processing unit, comprising

a decoder circuit selecting an instruction group corresponding to an inputted instruction code, based on a history of the inputted instruction code, and uniquely determining an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code, and

wherein said decoder circuit comprises:

a code linkage part linking a group code set based on a history of the inputted instruction code with the inputted instruction code, and outputting as an internal instruction code;

an internal decoder part determining an instruction to be executed in accordance with an internal instruction code to be supplied; and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups in advance of program execution, each instruction group is given with a group code different from others, each instruction is given with an instruction code different from others within the same instruction group and each instruction group having a certain instruction code to which an instruction belonging to another instruction group can be assigned, and said decoder circuit outputting a control signal corresponding to the instruction assigned to the certain instruction code to a processor element, when said certain instruction code is inputted.

12. (Previously presented) The information processing unit according to claim 11, wherein the instruction, which belongs to another instruction group and is assigned to the certain instruction code, is changeable .

13. (Previously presented) The information processing unit according to claim 11, wherein each of the instruction groups has a plurality of the certain instruction codes to which an instruction belonging to the other instruction group can be assigned.

14. (Currently amended) An information processing unit, comprising

a decoder circuit retaining information corresponding to a history of inputted instruction codes, selecting an instruction group corresponding to an inputted instruction code based on

the information, and uniquely determining an instruction to be executed selected from a plurality of executable instructions in accordance with the inputted instruction code, and

wherein said decoder circuit comprises:

a code linkage part linking a code concerning said information with the inputted instruction code, and outputting as an internal instruction code;

an internal decoder part determining an instruction to be executed in accordance with an internal instruction code to be supplied; and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups in advance of program execution, each instruction is given with an instruction code different from other instruction codes within the same instruction group and said decoder circuit temporarily changes the information when a certain instruction code is inputted.

15. (Currently amended) The information processing unit according to claim 14, wherein said decoder circuit determines an instruction to be executed based on ~~the inputted~~ a global instruction code only, irrespective of the information corresponding to the history of instruction codes, when the global instruction code is inputted .

16. (Currently amended) An information processing unit executing an instruction determined in accordance with an inputted instruction code,

comprising a decoder circuit retaining information corresponding to an input history of a plurality of inputted instruction codes, and uniquely determining an instruction to be executed selected from a plurality of instructions which are assigned to the inputted instruction code in advance of program execution, in accordance with a combination of the information and the inputted instruction code.

17. (Currently amended) The information processing unit according to claim 16, wherein the decoder circuit determines an instruction to be executed selected from a plurality of executable instructions, and the plurality of executable instructions are sorted into a plurality of instruction groups in advance of program execution, and each instruction is given with an instruction code different from others within the same instruction group.

18. (Currently amended) The information processing unit according to claim 16, wherein said decoder circuit determines an instruction to be executed, based on ~~the inputted~~ a

global instruction code only, irrespective of the information corresponding to the history of instruction codes, when the global instruction code is inputted.

19. (Currently amended) An information processing unit, comprising a plurality of processors on one chip, each processor capable of executing instructions independently, wherein each of said processors comprises:

a decoder circuit uniquely determining an instruction to be executed selected from a plurality of executable instructions based on an inputted instruction code and a group code corresponding to a history of the inputted instruction codes, and

a processor element executing an operation corresponding to a control signal provided from said decoder circuit, and

wherein said decoder circuit comprises:

a code linkage part linking said group code with the inputted instruction code, and outputting as an internal instruction code;

an internal decoder part determining an instruction to be executed in accordance with an internal instruction code to be supplied; and

wherein said plurality of executable instructions are sorted into a plurality of instruction groups assigned by the group code in advance of program execution, each instruction is given with an instruction code different from others within the same instruction group and the executable instruction includes an alias instruction to which an instruction belonging to the other instruction group can be assigned in advance to an internal instruction code.

20. (Previously presented) The information processing unit according to claim 19, wherein each of said processors further comprises a group register storing the group code, which is set up based on the history of the inputted instruction code.

21. (Previously presented) The information processing unit according to claim 20, wherein each of said processors further comprises a lookup table prescribing a change in a rule of the group code stored in said group register.

22. (Previously presented) The information processing unit according to claim 21, wherein said lookup table is set up with a combination of an instruction mask for setting a mask bit, an instruction code for comparing the internal instruction code, and the changed group code.

23. (Currently amended) The information processing unit according to claim 11, wherein each instruction group is given with a group code which is different than the group codes from other groups in advance of program execution, and the group code corresponding to the inputted instruction code is determined based on the history of the inputted instruction code.

24. (Previously presented) The information processing unit according to claim 14, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group.

25. (Previously presented) The information processing unit according to claim 17, wherein the information corresponding to the history of inputted instruction codes is a group code for selecting said instruction group.